REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

Allowable Subject Matter

As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claims 3, 4, 7, 10, 14 and 20 of the present application.

Summary of the Response

Claims 1-20 are currently pending in the application and subject to examination.

In the Office Action mailed April 22, 2005, claims 12, 13, 15, and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,173,367 to Aleksic, et al. (hereinafter "Aleksic"). Claims 1-2, 5-6, 8-9, 11, 16 and 18-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,987,551 to Garrett, Jr. (hereinafter "Garrett"), in view of U.S. Patent No. 4,984,208 to Sawada, et al. (hereinafter "Sawada"). To the extent that the rejections remain applicable to the claims currently pending, Applicants hereby traverse the rejections, as follows.

Claims 12 and 17 Recite Patentable Subject Matter

With respect to claims 12 and 17, Applicants respectfully submit that Aleksic fails to disclose or suggest each and every element of the claimed invention. For example, Aleksic fails to disclose or suggest at least the combination of features of "setting up, in a storage circuit in which image data is stored, a range of an image area in which the image data is written and a range of an additional area which is adjacent to the image

area and in which <u>data other than the image data</u> is written, with information supplied to a memory space of said storage circuit as a parameter," "writing <u>the additional data other than the image data</u> from external into the additional area in said storage circuit according to a first write control signal," and "writing the image data at an address location of the image area in said storage circuit according to a <u>second write control signal</u>," as recited in claims 12 and 17 (emphasis added).

Aleksic discloses a system and method for using a data cache in a system with both 2D and 3D graphics applications. The video system receives a mode signal indicating whether a 2D or 3D application is to be used. Depending on the mode signal, the system is implemented either as a <u>unified cache</u>, capable of being accessed by two separate data access streams (supporting 2D graphics), or as <u>two independent caches</u>, each accessed by <u>one data access stream</u> (supporting 3D graphics). *See, e.g.,* column 2, lines 51 to 63 (emphasis added). In 3D graphics mode, the Z-client and the 3D destination client requests are provided (column 3, lines 37 to 39), and the system of Aleksic splits cache memory 114 into two portions, 114A and 114B. *See, e.g.,* column 4, lines 48-49; *see also* Figure 1. This allows for the different data types used to support 3D graphics to have dedicated caches to optimize their access. However, all different data types that are stored in split cache portions 114A and 114B disclosed in Aleksic <u>relate to the display of the 3D image and are, therefore, image data</u>. Aleksic states, "each visual element associated with 3D graphics needs not only its 3D shape information, but additional shading information, or Z data, reflection information, and the Z-plane information." Column 1, lines 59 to 64; *see also* column 1, line 64 to column 2, line 12. Thus, the Z-data that the Office Action cites as anticipating the "<u>data other than</u>

the image data" feature recited in claims 12 and 17, is actually "image data" in Aleksic.

Furthermore, nothing in Aleksic discloses or suggests "writing the additional data other than the image data . . .into the additional area . . . according to a first write control signal," and "writing the image data . . . into the image area . . . according to a second write control signal," as recited in claims 12 and 17 (emphasis added).

Nothing in Aleksic teaches or suggests at least these features of the present invention, as recited in claims 12 and 17. For at least these reasons, Applicants submit that claims 12 and 17 are allowable over the cited prior art.

Claims 1 and 16 Recite Patentable Subject Matter

With respect to claims 1 and 16, the Applicants respectfully submit that nothing in the cited prior art, taken alone or in combination, discloses or suggests at least the combination of features of "an area adjustment circuit which sets up an additional area adjacent to an area in which the image data are actually stored in a memory space of said storage circuit and storing therein additional data other than the image data, which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the additional data in the additional area, in response to the address and a read control signal supplied to said storage circuit, wherein the additional data are written in with an address of the additional area," as recited in claims 1 and 16 (emphasis added).

Garrett discloses a hardware generated cursor overlay system, which uses a small section of the non-displayed frame buffer memory to store the pixel pattern and a raster scan line synchronization architecture to insert the cursor pattern information into

the corresponding line pattern of the video display frame. Column 2, lines 50-56. The cursor data is accessed from the non-displayed segment of the memory during horizontal blank time preceding the raster scan of the video pattern data subject to cursor overlay. The video pattern data in the frame buffer and cursor data are arranged by scan or row line. Column 2, lines 57-68. The column location of the cursor pattern is defined by the computer and stored in a position counter to be synchronously incremented by pixel during the scan of the frame buffer line. At the appropriate count, the cursor data is logically combined with frame buffer pattern data to superimpose the cursor characteristics on top of the video pattern data. Column 4, line 58 to column 5, line 7.

Nothing in Garrett, however, discloses or suggests at least the combination of features of an "area adjustment circuit which sets up an additional area," "data other than the image data," and that "the additional data are written in with an address of the additional area," as recited in claims 1 and 16. As shown in Figure 2 of Garrett, the frame buffer is divided into displayed and non-displayed portions, each of which is of a fixed size. All data that is stored in the Garrett frame buffer is image data, with the cursor outline and pattern data (which is image data) stored in the non-display area, and superimposed over the displayed data when necessary to show the cursor.

The Office Action does not allege that Sawada corrects the above deficiencies in Garrett and Sawada does not, in fact, correct these deficiencies. Therefore, Applicants submit that the combination of the cited art fails to disclose or suggest each and every limitation recited in claims 1 and 16. For at least these reasons, Applicants submit that claims 1 and 16 are allowable over the cited prior art.

Claims 2, 5, 6, 8, 9, 11, 13, 15, 18 and 19 Recite Patentable Subject Matter

Each of claims 2, 5, 6, 8, 9, 11, 13, 15, 18 and 19 depends from one of allowable claims 1, 12 or 16. Therefore, each of claims 2, 5, 6, 8, 9, 11, 13, 15, 18 and 19 incorporates each and every limitation recited within claims 1, 12 or 16. Therefore, it is respectfully submitted that claims 2, 5, 6, 8, 9, 11, 13, 15, 18 and 19 are allowable over the cited art for at least the same reasons that claims 1, 12 and 16 are allowable.

Claims 3, 4, 7, 10, 14 and 20 Recite Patentable Subject Matter

As the Examiner indicated in the Office Action, claims 3, 4, 7, 10, 14 and 20 recite patentable subject matter.

Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants

hereby petition for an appropriate extension of time. The Commissioner is hereby

authorized to charge any fee deficiency or credit any overpayment associated with

this communication to Deposit Account No. 01-2300, referring to client-matter

number 024354-00001.

Respectfully submitted,

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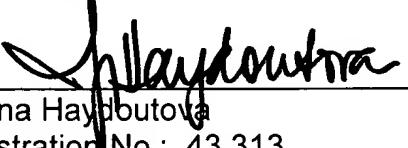
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